AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A register system for a data processing system comprising:

an unbanked memory unit having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to ~~at least~~ one specific register and processor mode;

input ports to receive inputs for addressing at least one of the memory locations using an encoded address;

output ports to output data from at least one of the memory locations addressable by an encoded address; and

a plurality of address encoders, a respective one of the plurality of address encoders for each of the input ports, each of the address encoders to provide an encoded address for accessing one of the memory locations, wherein each of the plurality of address encoders corresponds to only one of the input ports.

2. (Previously Presented) The register system of claim 1, wherein a plurality of registers correspond to the plurality of memory locations of the unbanked memory unit.

3. (Previously Presented) The register system of claim 2, wherein each register is addressable by a corresponding encoded address.

4. (Previously Presented) The register system of claim 3, wherein at least two registers are capable of being accessed in different processor modes using the same encoded address.

5. (Previously Presented) The register system of claim 1, wherein the plurality of memory locations are discontinuous in the unbanked memory unit.

6. (Previously Presented) The register system of claim 1, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

7. (Previously Presented) The register system of claim 2, wherein inputs are received associated with at least one register and processor mode, and wherein at least one of the outputs is data from a register associated with an encoded address obtained from the received inputs.

8. (Previously Presented) The register system of claim 7, wherein data is outputted from the unbanked memory unit for at least two instructions.

9. (Previously Presented) The register system of claim 2, wherein inputs are associated with at least one register and processor mode, and wherein one of the inputs is data to be written in a register associated with an encoded address obtained from the received inputs.

10. (Previously Presented) The register system of claim 9, wherein data for at least two retired instructions is to be written in at least two registers.

11. (Cancelled)

12. (Previously Presented) The register system of claim 1, further comprising:

latches to latch an encoded address from respective ones of the address encoders; and

selectors coupled to respective ones of the latches and the address encoders, the selectors to select the encoded address from either the latches or the address encoders.

13. (Previously Presented) The register system of claim 10, wherein the latches store the encoded address as a pipeline storage of the encoded address.

14. (Currently Amended) A register system for a data processing system comprising:

unbanked memory means having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to ~~at least~~ one specific register means and processor mode;

a plurality of input means to receive inputs for addressing at least one of the memory locations using an encoded address;

output means to output data from at least one of the memory locations addressable by an encoded address; and

a plurality of addressing means, one of the addressing means for each of the input means, each of the addressing means to provide an encoded address for accessing one of the memory locations, wherein each of the plurality of addressing means corresponds to only one of the plurality of input means.

15. (Previously Presented) The register system of claim 14, wherein a plurality of register means correspond to the plurality of memory locations of the unbanked memory means.

16. (Previously Presented) The register system of claim 15, wherein each register means is addressable by a corresponding encoded address.

17. (Previously Presented) The register system of claim 16, wherein at least two register means are capable of being accessed in different processor modes using the same encoded address.

18. (Previously Presented) The register system of claim 14, wherein the plurality of memory locations are discontinuous in the unbanked memory means.

19. (Previously Presented) The register system of claim 14, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

20. (Previously Presented) The register system of claim 16, wherein inputs are received associated with at least one register means and processor mode, and wherein at least one of the outputs is data from a register means associated with an encoded address obtained from the received inputs.

21. (Previously Presented) The register system of claim 20, wherein data is outputted from the unbanked memory means for at least two instructions.

22. (Previously Presented) The register system of claim 15, wherein inputs are associated with at least one register means and processor mode, and wherein one of the inputs is data to be written in a register means associated with an encoded address obtained from the received inputs.

23. (Previously Presented) The register system of claim 22, wherein data for at least two retired instructions is to be written in at least two register means.

24. (Cancelled)

25. (Previously Presented) The register system of claim 14, further comprising:

a plurality of latching means to latch an encoded address from respective ones of the addressing means; and

a plurality of selecting means coupled to respective ones of the latching means and the addressing means, the selecting means to select the encoded address from either the latching means or the addressing means.

26. (Previously Presented) The register system of claim 23, wherein the latching means stores the encoded address as a pipeline storage of the encoded address.

27-50. (Cancelled)

51. (Currently Amended) A processor comprising:

an integrated circuit including:

an unbanked memory unit having input ports for addressing a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to ~~at least~~ one specific register and processor mode; and

a plurality of address encoders to provide at least one encoded address for addressing at least one of the memory locations, wherein each of the plurality of address encoders corresponds to only one of the input ports.

52. (Previously Presented) The processor of claim 51, wherein a plurality of registers correspond to the plurality of memory locations in the unbanked memory unit.

53. (Original) The processor of claim 52, wherein each register is addressable by a corresponding encoded address.

54. (Original) The processor of claim 53, wherein at least two registers are capable of being accessed in different processor modes using the same encoded address.

55. (Previously Presented) The processor of claim 51, wherein the plurality of memory locations are discontinuous in the unbanked memory unit.

56. (Original) The processor of claim 51, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

57. (Original) The processor of claim 51, wherein each address encoder includes input ports to receive inputs associated with at least one register and processor mode in providing a corresponding encoded address.

58. (Original) The processor of claim 57, wherein each address encoder includes logic circuitry to obtain the corresponding encoded address based on the received inputs.

59. (Original) The processor of claim 58, wherein the logic circuitry includes at least one of a programmable gate array (PGA) or a field programmable gate array (FPGA).

60. (Original) The processor of claim 51, wherein the processor is at least one of an embedded processor and a microprocessor.

61. (Currently Amended) A data processing system comprising:

a memory mapped register system for accessing a plurality of memory locations via input ports, each memory location being addressable by an encoded address, wherein the encoded address corresponds to ~~at least~~ one specific register and processor mode; and

a plurality of address encoders, a respective one of the plurality of address encoders for each of a plurality of input ports of the register system, each of the address encoders to provide an encoded address for accessing one of the memory locations, wherein each of the plurality of address encoders corresponds to only one of the input ports.

62. (Original) The data processing system of claim 61, wherein a plurality of registers correspond to the plurality of memory locations.

63. (Original) The data processing system of claim 62, wherein each register is addressable by a corresponding encoded address.

64. (Currently Amended) A processor comprising:

circuit means including:

unbanked memory means having input means for addressing a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to ~~at least~~ one specific register means and processor mode; and

a plurality of addressing means to provide at least one encoded address for addressing at least one of the memory locations, wherein each of the plurality of addressing means corresponds to only one of the input means.

65. (Previously Presented) The processor of claim 64, wherein a plurality of register means correspond to the plurality of memory locations of the unbanked memory means.

66. (Original) The processor of claim 65, wherein each register means is addressable by a corresponding encoded address.

67. (Original) The processor of claim 66, wherein at least two register means are capable of being accessed in different processor modes using the same encoded address.

68. (Previously Presented) The processor of claim 64, wherein the plurality of memory locations are discontinuous in the unbanked memory means.

69. (Original) The processor of claim 64, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

70. (Original) The processor of claim 64, wherein each addressing means includes input means to receive inputs associated with at least one register means and processor mode in providing a corresponding encoded address.

71. (Original) The processor of claim 70, wherein each addressing means includes logic means to obtain the corresponding encoded address based on the received inputs.

72. (Original) The processor of claim 71, wherein the logic means includes at least one of a programmable gate array (PGA) or a field programmable gate array (FPGA).

73. (Original) The processor of claim 64, wherein the processor is at least one of an embedded processor and a microprocessor.

74. (Currently Amended) An integrated circuit method comprising:

configuring the integrated circuit to receive a plurality of inputs;

configuring the integrated circuit to determine an unbanked encoded address based on the received inputs, wherein the unbanked encoded address corresponds to ~~at least~~ one specific register and processor mode;

receiving the plurality of inputs from a plurality of address encoders;

configuring the integrated circuit to access a register via a corresponding one of a plurality of input ports using an unbanked encoded address; and

configuring the integrated circuit to output data from the accessed register, wherein each of the plurality of address encoders corresponds to only one of the plurality of input ports.

75. (Original) The method of claim 74, further comprising:

configuring the integrated circuit to output data for multiple instructions.

76. (Original) The method of claim 74, further comprising:

configuring the integrated circuit to write data to the accessed register.

77. (Original) The method of claim 76, further comprising:

configuring the integrated circuit to write data to one or more accessed registers for multiple executed instructions.

78. (Currently Amended) A method for accessing an unbanked memory unit having a plurality of memory locations comprising:

receiving a memory request for accessing the unbanked memory unit at one of a plurality of address encoders, the memory request including a register index input and a processor mode input;

encoding the register index input and processor mode input at the one of the plurality of address encoders to obtain an encoded address;

accessing at least one of the memory locations of the unbanked memory unit via input ports in accordance with the encoded address, wherein the encoded address corresponds to at least one register and processor mode; and

writing data into or reading data from the accessed memory location, wherein each of the plurality of address encoders corresponds to only one of the input ports.

79. (Original) The method of claim 78, wherein writing data into or reading data from the accessed memory location includes writing data into or reading data from the accessed memory location for multiple instructions,

80-85. (Cancelled)